REMARKS

The present amendment is being filed in response to the Official Action dated May 21, 2003, wherein the Examiner rejected pending claims 1, 5-16, 29, 31-34 and 38-41. More specifically, claims 1, 9-10 and 29 are rejected as being anticipated by Iimura et al., EP Published Patent Application No. 0,446,855; claims 5-8, 11-16 and 31 are rejected as being unpatentable over Iimura et al., '855, in view of Yokoyama et al., US Patent No. 5,678,060; claims 32-34 are rejected as being unpatentable over Iimura et al., '855, in view of Zampini et al., US Statutory Invention Registration No. H1752; and claims 38-41 are rejected as being unpatentable over Iimura et al., '855, in view of Grant et al., US Patent No. 4,805,137. However, contrary to the assertions by the Examiner Iimura et al., '855, either alone or in various combination with the other references being relied upon by the Examiner fail to make known or obvious the claims of the present application.

More specifically, contrary to the Examiner's assertions, Iimura et al., '855, which serves as the base reference for all of the Examiner rejections, fails to provide for a direct memory access module/controller, which selectively establishes a direct memory access data transfer channel between a plurality of nodes, such as a plurality of peripheral interfaces, and both a first memory, and a second memory.

While Iimura et al., '855, includes both a main memory 3, coupled to a system bus 5; and a memory module 11, coupled to a common internal bus 12, it can not be fairly said that any direct memory access data transfer channels are established between the memory module 11 (and/or the associated bus/processor interface) and any of the plurality of nodes, such as a plurality of peripheral interfaces, as provided by respective ones of the claims in the present application, such that the corresponding claimed features in the claims of the present application could be said to be either anticipated or made obvious by the cited reference. While the DMA control circuit 9, in Iimura et al., '855, is identified as transferring data not via the host processor 4, but directly to the main memory 3 (col. 4, lines 38-41), no such corresponding functionality is associated with memory module 11. Alternatively, memory module 11 is identified as storing various control data such as system constants needed for controlling the data transfer and also various control information necessary for controlling the data transfer under DMA control (col. 4, lines 42-47). In effect, the memory module 11, in conjunction with CPU 10, manages the

operation of the communication processing system, and there is no indication that they serve as either a source or destination of any information communicated via a direct memory access data channels.

As a result, Iimura et al., '855, contrary to the Examiner's assertions, does not include both a first memory and a second memory, wherein the programmable direct memory access module selectively configures the programmable direct memory assess data channel between each of the first memory and the second memory, and respectively, each one of the plurality of nodes (claims 9 and 12)/ peripheral interfaces (claim 1). Similarly Iimura et al., '855, fails to be operable for establishing multiple data transfers between both a first processor direct memory access interface and a second processor direct memory access interface, and the one or more peripheral ports, as well as between each of the first and second processor direct memory access interfaces (claim 29).

The other pending claims (claims 5-8, 10, 11, 13-16, 31-34 and 38-41), which are each dependent upon one of the independent claims (claims 1, 9, 12 or 29) would each be allowable for at least the same reasons that each of the corresponding independent claims are identified, above, as being allowable. Consequently, each of the dependent claims are neither anticipated nor made obvious by the various combinations of references being cited by the Examiner. Furthermore, none of the other references account for the deficiency noted above with respect to Iimura et al., '855.

The applicants contend that the claims, as presently amended, are allowable over the prior art of record, for the reasons noted above. Allowance of the application is therefore respectfully requested. Should any issues remain unresolved after the consideration of the present response, the Examiner is invited to contact the applicant's representative at the number listed below to discuss the same.

Respectfully submitted,

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